# Assignment 3: Exploring Memory Hierarchy Design in gem5

## Assignment Objectives and Goals

The memory hierarchy, a crucial aspect of computer architecture, orchestrates the intricate dance between processor and storage. This assignment challenges you to go beyond textbook definitions and delve into the practical implications of memory hierarchy design using the gem5 simulator. You will navigate the landscape of memory technologies, experiment with cache optimizations, and witness the power of virtual memory in action. By the end of this assignment, you will have a deeper appreciation for the tradeoffs and design choices involved in crafting efficient and high-performance memory systems.

## Part 1: Understanding Memory Hierarchy

### 1. Introduction to Memory Hierarchy Design:

Reading Assignment: Read the provided sections on Memory Hierarchy Design, focusing on the key concepts of memory technology, cache optimizations, virtual memory, and design considerations.

**Conceptual Analysis and Discussion**

Write a 2-3 page document that articulates the significance of memory hierarchy design in achieving high-performance computing systems. Your analysis should consider the following key aspects:

* Memory Technologies

Explore the spectrum of memory technologies available today, from fast but expensive SRAM to slower but cost-effective DRAM and beyond. Analyze how the characteristics of these technologies influence their placement within the memory hierarchy and their impact on overall system performance.

* Advanced Cache Optimization

Beyond the basics of cache organization, delve into sophisticated techniques like prefetching, victim caches, and cache partitioning. Explain how these techniques aim to minimize cache misses and improve overall system throughput.

* Virtual Memory and Virtual Machines

Unravel the intricacies of virtual memory, including page tables, address translation, and page replacement algorithms. Discuss how virtual memory enables efficient memory management and supports the execution of multiple processes concurrently. Explore the concept of virtual machines and their relationship to the memory hierarchy.

* Cross-Cutting Issues

Address the challenges and trade-offs involved in designing memory hierarchies. Consider factors like cost, power consumption, complexity, and the impact of different workloads on performance. Discuss emerging trends and technologies that are shaping the future of memory hierarchy design.

## Part 2: Implementing and Analyzing Cache Configurations in gem5

### Introduction

In this hands-on section, you will leverage the power of the gem5 simulator to gain practical experience with memory hierarchy design principles. Specifically, you'll focus on the cache subsystem, which plays a crucial role in bridging the performance gap between the CPU and main memory. By setting up and running simulations, you'll witness firsthand how various cache configurations can influence system performance. Moreover, you'll explore the concept of virtual memory, a vital mechanism for efficient memory management in modern systems.

### Setting Up gem5:

Environment Setup: Follow the instructions to set up gem5, ensuring you have the latest version and necessary dependencies installed.

Carefully follow the gem5 installation instructions to set up the simulator on your system. Ensure you have the latest version of gem5 installed and all necessary dependencies are met. You may need to consult the gem5 documentation or online resources for guidance specific to your operating system.

**Configuration:** Configure gem5 to simulate a system with an x86 architecture. Pay particular attention to the cache subsystem settings, as this will be the focus of your experiments. Refer to the gem5 documentation for details on how to configure cache parameters such as size, associativity, and block size.

### Simulation of Cache Performance:

* D **Default Cache Configuration**

Begin by running a simulation using gem5's default cache settings. This will establish a baseline for comparison. Record essential performance metrics, including cache hit rate, miss rate, and average memory access latency.

* **Optimizing Cache Parameters**

Systematically modify various cache configuration parameters, such as cache size, associativity, and block size. For each modification, rerun the simulation and record the updated performance metrics. Aim to improve the overall cache performance, and carefully document the changes you make and their rationale.

* **Analysis**

Compare the performance metrics obtained before and after each optimization. Analyze how each change in cache configuration affected the results. Relate your observations to the advanced cache optimization techniques discussed in the theoretical part of the assignment (e.g., prefetching, victim caches).

### Virtual Memory Exploration:

4. Virtual Memory Exploration:

* Virtual Memory Simulation

Configure gem5 to simulate a system with virtual memory enabled. Experiment with different page sizes and Translation Lookaside Buffer (TLB) configurations.

* Performance Metrics

Analyze the performance impact of your virtual memory configuration choices. Focus on metrics such as page fault rate and TLB miss rate, and how these influence overall system performance.

* Hands-On Discussion

Reflect on the role of virtual memory in modern operating systems and how TLB configurations can impact system performance. Connect your experimental findings to the theoretical concepts you've learned about virtual memory management.

Remember:

* Document your experimental setup, including the benchmark program used, gem5 configuration details, and any modifications made.
* Use clear and well-labeled graphs or tables to present your performance data.
* Provide insightful analysis, explaining the observed trends and relating them to theoretical principles.
* Store all files and documents in a private github repository and ensure that your professor is the only person with access to the repository.

## Submission:

* Deliverables:

Submit appropriate documents for parts 1 and parts 2.

Include screenshots of your gem5 simulation outputs, configuration files, and any graphs or charts used to present data and a link to your github repository.

## Evaluation Criteria:

* Discussion on Memory Hierarchy Considerations: Appropriate and detailed Memory Hierarchy Discussion
* Programming and Development Accuracy: Correct execution of the "Hello World" program in gem5.
* Screenshots: Report accurately provides screenshots depicting output and each step.
* Documentation and APA Guidelines: Clarity and completeness of the report.
* Troubleshooting: Appropriate discussion and documentation on the ability to identify and resolve issues encountered during the process